Listing of the claims:

Please amend claims 1-3 and add claims 13-19 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A thin film Silicon on Insulator (SOI) device comprising:

a source;

a gate;

a drain;

an SOI layer;

a substrate layer~~; an insulator layer between the SOI layer and the substrate layer~~, wherein when the substrate layer is maintained at a potential sufficiently lower than a potential of the source a parasitic MOS channel is formed between the source and drain; and

a Deep N implant layer formed between either the source or drain and the SOI ~~insulator~~ layer to prevent flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. (Currently amended) The device of claim 1 wherein the Deep N implant layer is formed between the source and the SOI ~~insulator~~ layer.

3. (Currently amended) The device of claim 1 wherein the Deep N implant layer is formed between the drain and the SOI ~~insulator~~ layer.

4-11. (Cancelled).

12. (Previously presented) The device of claim 1, wherein the substrate layer is maintained at a potential that is about 200 volts lower than the potential of the source.

13. (New) The device of claim 1, wherein the SOI layer has a thickness of about 1 micron.

14. (New) The device of claim 1, wherein the Deep N implant layer has a doping concentration about 1 order of magnitude higher than that of a gate region associated with the gate.

15. (New) A thin film Silicon on Insulator (SOI) device comprising:

a source and a drain;

a gate between the source and the drain to control on and off states of the device;

a substrate layer;

a deep implant layer adjacent to either the source or the drain; and

an SOI layer disposed between the substrate layer and the deep implant layer,

wherein when the substrate layer is maintained at a potential sufficiently different than a potential of the source, a parasitic MOS channel is formed between the source and drain, and wherein the deep implant layer prevents flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

16. (New) The device of claim 15, wherein the deep implant layer is formed between the source and the SOI layer.

17. (New) The device of claim 15, wherein the deep implant layer is formed between the drain and the SOI layer.

18. (New) The device of claim 15, wherein the deep implant layer is a Deep P implant layer.

19. (New) The device of claim 15, wherein the deep implant layer is a Deep N implant layer.